

Implementation of CMOS Phase and Quadrature Differential Oscillators through Delay Lines

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Abstract

Some of the most important aspects in ICs is the portability and power consumption of implemented systems. In this view are placed CMOS Phase and Quadrature Pulsed Oscillators. This oscillator architecture is indicated when the project requirements aim to high performance in terms of phase noise with limited energy expended.

The object of this work is an innovative solution to design coupled oscillators systems through the use of electromagnetic structures, e.g. microstrip waveguides used to introduce a finite phase delay. In the first part of the project, in order to obtain an architectural analysis of the oscillator, the delay line is simulated by transmission lines. Line parameters are obtained according to the process constraints. In this place are found solutions for buffering and driving issues. Next, the analysis is extended toward integration of the TEM waveguide in chip back-end. The choice of a microstrip allows to use the metallization layers as a delay electromagnetic structure. To improve the integration of the system we need to fall back the microstrip getting meanders and to reduce the radiation loss of the waveguide we need to smooth the corners (Fig. 1). In this step the algorithms for design of waveguides are implemented.

Results of this work are:

- an innovative oscillator architecture
- integrable waveguides, with single guide occupation less than 10% of the inductor area
- high phase noise performance (Fig. 2) with energy consumption improvement less than 50% with respect to the reference oscillator, due to the pulsed architecture.
FOM improvement 4.0 dB
- the fulfillment of foundry specifics

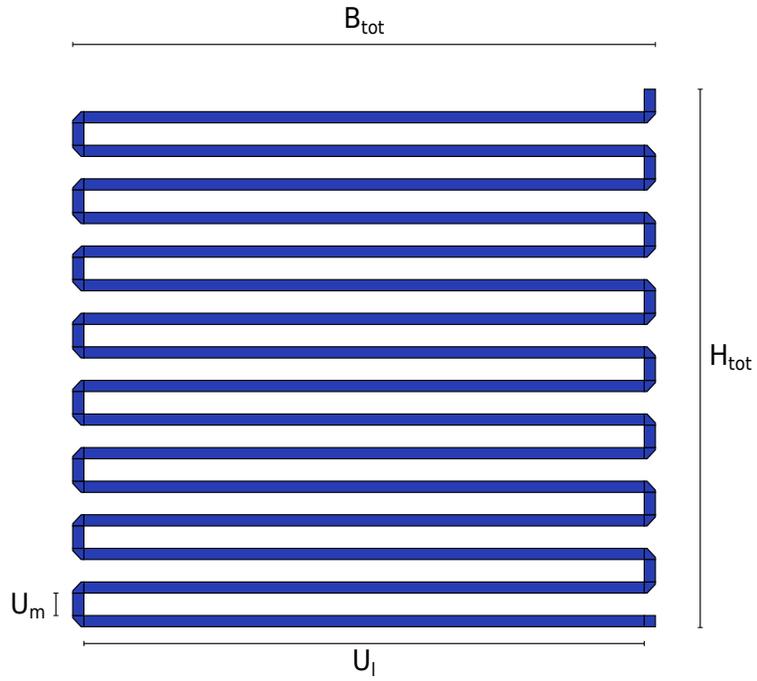


Figure 1: Layout of the proposed 8-meander folded microstrip delay line

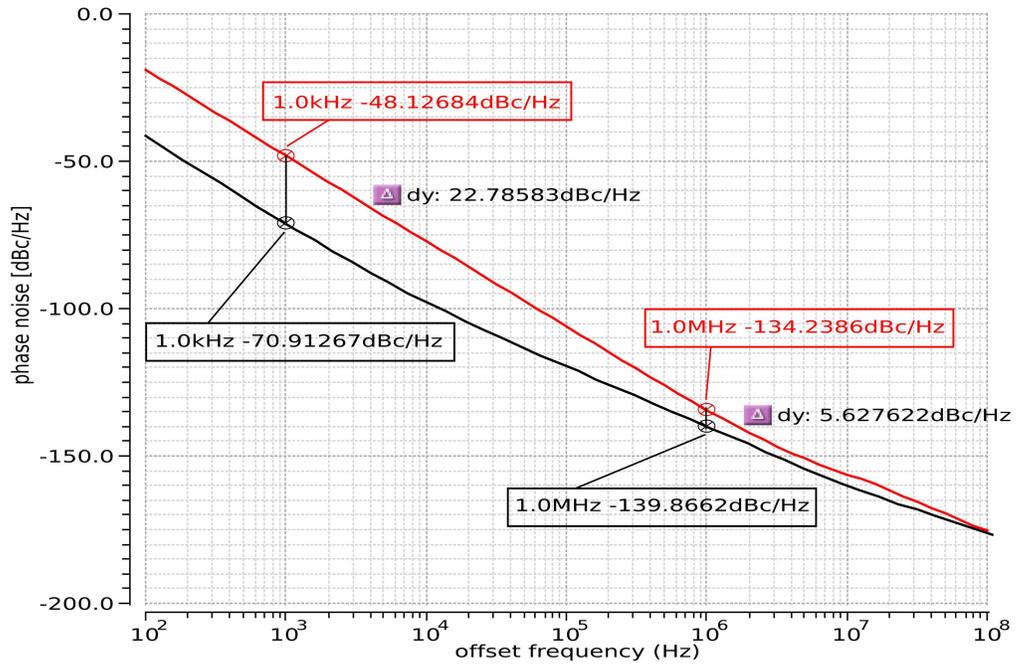


Figure 2: Phase Noise results

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